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EXAMINER
NGUYEN, HA T

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/829,161	Applicant(s) AKRAM, SALMAN
	Examiner Ha T. Nguyen	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 72-106* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 72-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Notice to applicant

1. Applicants' Amendment and Response to the Office Action mailed 4-25-02 has been entered and made of record (Paper No. 11).

Response to Amendment

2. In view of Applicant' s amendment to the claims, the rejection of claims 81 and 87 under 35 U.S.C. 112 second paragraph, has been withdrawn.

In view of new art found, the allowability of claims 25, 26, 76, and 77 has been withdrawn.

In view of Applicant' s arguments and the amendment to the claims, the rejections of claims 1, 3, 5, 7-10, 14, 22, 72-74, 79, 80, 83-87, 92, and 100 under 35 U.S.C. 102(e) and 2, 4, 6, 15-21, 23, 24, 78, 81, 82, 93-99, 101, and 102 under 35 U.S.C. 103(a), as being anticipated by or unpatentable over Kim (U. S. Patent 6020233), have been withdrawn.

Applicants' arguments with regard to the rejections under 35 U.S.C. 103, as being unpatentable over Liu et al. (US Patent 6277745, hereinafter "Liu") have been fully considered, but they are not deemed to be persuasive for at least the following reasons. Applicant argued that the barrier layer 8 in Liu is not conducting metal, the examiner disagrees, TaN, TiN are conducting materials containing metal and Ta is a metal. Through out the specification and claims applicants refer to metal layer as layer containing Ta, Ti, W, TaN, TiN, TiW, WN, or TaN (see for example page 8, paragraphs 0031 and 0032) since some of the cited materials are metals some are metal containing materials which are conductive materials, Liu's layer 8 meets the claimed limitation "conducting layer" of claim 1.

Applicant argued that Liu fails to expressly or inherently disclose a single conductive layer as recited in claim 1, the examiner disagrees, the claim language " comprising" allows for other conductive layer to be formed above or below the claimed single conducting layer which result in practically not a single conducting layer. In other word, the limitation "single" does not really limit further the limitations of the claim.

Besides, Applicant argued that Liu "discloses forming a hard mask 16 over the second metal barrier layer 8" and not a second dielectric layer. The examiner disagrees, Liu discloses

that the hard mask is of dielectric material polyimide, SiO2 or Si3N4 or SiON, therefore Liu's hard mask layer 16 meets the "second dielectric" limitation of the claim.

Therefore, Liu does make obvious the limitations of claims 1 and 11-13.

Specification

3. The specification is objected to for containing the following informality: through out the specification the use of metal layer to mean metal containing layer or conducting layer is not correct because Ta, Ti, W are metals but TaN, TiN, TiW, WN, or TaN are metal containing or conductive layer (see for example page 8, paragraphs 0031 and 0032). Correction is required.

Note that applicant did not argued against the examiner's Official Notice concerning a dielectric layer formed on a substrate and polyimide and fluorine-doped silicon oxide being low k alternatives used in the fabrication of a semiconductive device, this is considered as an admission of prior art.

Claim Objections

4. Claims 1-26 and 72 -102 are objected to because of the following informalities: in claims 1 and 72, lines 9 and 7, respectively, the use of "metal spacer" is incorrect, it should be -- conducting spacer-- or --metal containing spacer-- because claims 9 and 85 specify TiN, TaN, and other metal compounds to be the material for the "metal spacer", this is also true for other claims having this limitation, there are so many, it is not possible to point them out all. Appropriate correction is required.

Claims 2-26 and 72-102 variously depend from claim 1 or 72, they are objected for the same reason.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11, 14-26, 72-89, and 92-106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (U. S. Patent 6030896).

[Claims 1, 72-75, and 87] Referring to Figs. 1-5 and related text, Brown discloses a method of fabricating a semiconductor device, comprising the steps of: forming a substantially planar first dielectric layer 10 on a substrate (see col. 4, lines 11-13); forming at least one metal containing layer 12, 14 over the first dielectric layer; forming a single conducting layer 16 or 18 over the at least one metal containing layer; forming a second dielectric layer over the single conducting layer (see col. 4, lines 50-62); removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form a multilayer structure (see Fig. 2); and forming metal containing spacers 22 on sidewalls of the multilayer structure, said metal containing spacers being substantially the same height as said multilayer structure (see Fig. 3). But it does not disclose expressly that the spacer is of metal. However, the missing limitation is well known in the art because Brown also discloses that Ta, Ti, TaN, and TiN are equivalently used diffusion barrier material (See col. 4, lines 15-19) .

[Claims 2 and 78] wherein said forming the first dielectric layer comprises forming a silicon oxide or BPSG layer (see col. 4, lines 11-14);

[Claims 3, 5, 79, and 80] wherein said forming the at least one metal containing layer comprises forming the at least one metal layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN and wherein said forming the at least one metal containing layer comprises forming the at least one metal layer of titanium or titanium nitride (see col. 4, lines 15-18);

[Claims 4 and 81] further comprising forming a second metal layer 12 between a first metal containing layer 14 of said at least one metal containing layer and the substrate, said second metal containing layer comprising TiN, TiW, WN, or TaN (see col. 4, lines 13-19);

[Claims 6 and 82] wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer of titanium or titanium nitride (see col. 4, lines 13-19];

[Claims 7 and 83] wherein said forming the single conducting layer 14 or 18 comprises forming the conducting layer from at least one of aluminum and copper (see col. 4, lines 32-49] ;

[Claims 8 and 84] Brown does not teach wherein said forming the conducting layer comprises forming the conducting layer of an aluminum-copper alloy. However the examiner takes Official Notice that aluminum-copper is a conventional conducting material used in semiconductor device when lower cost and ease of fabrication are desirable.

[Claims 9, 10, 85 and 86] wherein said forming the metal containing spacers comprises forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN ; wherein said forming the metal containing spacers comprises forming the metal spacers of titanium or titanium nitride (see col. 4, line 11-col. 5, line 5);

[Claims 11 and 89] wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal spacers to extend along the sidewalls of the second dielectric layer (see Fig. 2 and col. 4, lines 50-62);

[Claims 14 and 92] further comprising forming the at least one metal layer and the metal spacers of a same metal, in the case where the layer 12 is formed of TiN or TiN (see col. 4, lines 15-18 and 63-67);

[Claims 15-18, and 93-96] Brown discloses substantially the limitations of claims 15-18, and 93-96, as shown above. But Brown does not discloses the method of deposition the at least one metal layer and the single conducting layer. However, it would have been obvious for a person of ordinary skill in the art to use CVD to deposit the layers to have the same method of deposition as the metal containing spacer layers to obtain conformal layers and to reduce the equipment requirements (see par. bridging cols. 4 and 5);

[Claims 19, 20, 97, and 98] wherein said forming the metal containing spacers comprises forming the metal containing spacers by CVD, vapor deposition and directional etching (see par. bridging cols. 4 and 5);

[Claims 21 and 99] wherein removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form a multilayer structure id effected by patterning and etching the second dielectric layer, single conducting layer, and at least one metal containing layer (see col. 4, lines 50-62);

[Claims 22-24, 88, 100-103, and 105] wherein said forming the metal spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers; wherein said forming the metal spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer by conformal deposition process; wherein portions of the metal spacer layer over the multilayer structure and first dielectric layer are removed by etching (See par. bridging cols. 4 and 5);

[Claims 25, 26, 76, 77, 104, and 106 further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto (see Fig. 5); by etching (see col. 5, lines 18-33);

[Claims 75 and 87]wherein flanking at least one surface of the multilayer structure with a metal spacer comprises forming a metal containing spacer 22 layer on said second dielectric layer or on sidewalls of said multilayer structure (see Fig. 3 and par. bridging cols. 4 and 5).

Therefore, it would have been obvious to use Brown's teaching to obtain the invention as specified in claims 1-11, 14-26, 72-89, and 92-106.

7. Claims 1, 11-13, 72-75, and 88-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al., U. S. Patent 6277745 (Hereinafter Liu).

[Claims 1 and 72-75] Referring to Figs. 2A-2F and related text, Liu discloses a method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer 2 (see col. 3, lines 31-35); forming at least one metal containing layer 4, 6 over the first dielectric layer; forming a single conducting layer 8 over the at least one metal containing layer; forming a second dielectric layer 16 over the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form a multilayer structure (see Fig. 2B); and forming metal spacers on sidewalls of the multilayer structure, said metal spacers being substantially the same height as said multilayer structure (see Fig. 2D); wherein flanking at least one surface of the multilayer structure with a metal spacer comprises forming a metal spacer 12 layer on said second dielectric layer (see Fig. 2C and col. 4, lines 20-67). But it does not disclose

expressly that the first dielectric layer is formed on a substrate. However, the examiner takes Official Notice that it is well known in the art that a dielectric layer is formed on a substrate.

[Claims 11 and 89] Liu also discloses wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the conducting layer (see Fig. 2B), and forming the metal spacers to extend along the sidewalls of the second dielectric layer (see Fig. 2D); and

[Claims 12 and 90]; further comprising forming the second dielectric layer of a low dielectric constant material (see col. 5, lines 1-5).

[Claims 13 and 91] Liu discloses substantially the limitations of claims 13 and 91, as shown above. But it does not disclose expressly that the second dielectric layer is of fluorine-doped silicon oxide. However, the examiner takes Official Notice that it is well known in the art that polyimide and fluorine-doped silicon oxide are low k alternatives used in the fabrication of a semiconductive device .

Therefore, it would have been obvious to use Liu' s teaching to obtain the invention as specified in claims 1, 11-13, 72-75, and 88-91.

8. Claims 1-12, 14-24, 72-75, 78-90, 92-102 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brenna et al. (U.S. Patent 6074943, hereinafter "Brenna") .

[Claims 1-3, 5-11, 14,19-24 and 72-75, 78-80, 82-89, 92, 97-102] Referring to 2A-2H and related text, Brenna discloses a method for making a metallization structure for a semiconductor device, comprising: forming a first dielectric layer 200 of silicon oxide; forming at least one metal containing layer 205 of TiN, 210 over the first dielectric layer (see col. 2, lines 37-42); forming a single conducting layer 215 over the at least one metal containing layer; forming a second dielectric layer 220 over the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form a multilayer structure (see Fig. 2D); and forming metal spacers 240 of TiN on sidewalls of the multilayer structure, said metal spacers being substantially the same height as said multilayer structure (see Fig. 2F and col. 3, lines 28-34, col. 4, lines 32-58); wherein flanking at least one surface of the multilayer structure with a metal spacer comprises forming a metal spacer 240 layer on said second dielectric layer (see Fig. 2E, 2F and col. 2, lines 51-58).

But it does not disclose expressly that the first dielectric layer is formed on a substrate and it is substantially planar dielectric. However, the examiner takes Official Notice that it is well known in the art that a dielectric layer is formed on a substrate.

[Claims 4 and 81] when 210 is the at least one metal containing layer then 205 is the second metal containing layer of TiN

[Claims 12 and 90] Forming second dielectric layer of low dielectric constant (see col. 6, lines 33-39).

[Claims 15-18, and 93-96] Brenna discloses substantially the limitations of claims 15-18, and 93-96, as shown above. But Brown does not discloses the method of deposition the at least one metal layer and the single conducting layer. However, it would have been obvious for a person of ordinary skill in the art to use CVD to deposit the layers to have the same method of deposition as the metal containing spacer layers to obtain conformal layers and to reduce the equipment requirements (see par. bridging col. 2, lines 51-58).

Therefore, it would have been obvious to combine with to obtain the invention as specified in claims 1-12, 14-24, 72-75, 78-90, 92-102.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha Nguyen whose telephone number is (703)308-2706 . The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308-3325. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Ha Nguyen
Primary Examiner
10 - 04 - 02